REMARKS

The above-referenced patent application has been reviewed in light of the Office Action of March 20, 2003. Reconsideration of the above-referenced patent application in view of the amendments and remarks is respectfully requested.

Claims 2-9, 13, 14 and 16-19 are pending in the above-referenced application.

RESPONSE TO 35 U.S.C. §102 REJECTION

The Examiner rejected claim 19 under 35 USC 102(b) as anticipated by Gannett (U.S. Patent No. 5,790,130). In particular, Applicant respectfully disagrees with the Examiner's assertion. In particular, Gannett fails to teach or suggest a "cache controller transferring texture data at the main memory access granularity" as claimed in claim 19 and the claims that depend therefrom. In particular, pre-fetching efficiency is maximized by texel block granularity being the same or substantially the same as memory bus granularity. The present invention provides for.

As noted in the specification on page 7, paragraph 3, the present invention provides for:

> "d) minimization of the texture data fetch granularity to the memory bus width to minimize speculative prefetch penalties and maximize the use of limited local storage for use and reuse of data stored."

Also, as noted on page 9, line 8 to page 10, first paragraph:

> "A labeling scheme on a larger scale using one fetch unit of multiple texels as a block each having a separate identifier is also described. In the bilinear interpolation case, the preferred embodiment will include four separate texel block identifiers, where each block consists of one each of the block identifier. The texture cache memory is partitioned into a plurality of rows corresponding to a block texel identifier. Each cache memory bank has at least one row corresponding to each block identifier. In this embodiment, this partitioning of data allows the cache controller to be broken into four smaller controllers. **In this case, the least significant bits of U and V texture block addresses at the fetch granularity are used to determine the type of texel blocks needed.** Once the particular texel block is determined, the respective cache controller determines if the block is in cache or is needed to be fetched from main memory.

> The present invention provides a unique method of viewing texture data in memory that is optimized for bilinear interpolation filtering texture. The memory organization scheme is extendable to handle trilinear interpolation or multiple texture maps through a duplication of the cache hardware. The tailored hierarchical texture cache scheme greatly reduces memory accesses while holding cache misses to a minimum. The scheme allows for minimal cache storage requirements. **The present invention maximizes prefetching efficiency by the texel fetch granularity being the same as memory bus width granularity.**" (Emphasis added.)

Gannett fails to teach or suggest cache controller transferring texture data at the main memory access granularity. In particular, the passages cited by the Examiner (column 21 lines 55-64 and column 22 lines 9-15) fail to teach or suggest this aspect. Gannett merely alludes to transferring data to main memory and fails to teach the texel fetch granularity being the same or substantially the same as the memory bus width granularity.

RESPONSE TO 35 U.S.C. §103 REJECTION

The Examiner rejected claims 2-10, 13-14, 16-17 under 35 U.S.C. §103(a) as being unpatentable over Gannett. This rejection of these claims on this basis is traversed. In particular, Gannett fails to teach or suggest a "cache controller transferring texture data at the main memory access granularity" for the reasons noted above.

RESPONSE TO 35 U.S.C. §102 REJECTION

The Examiner rejected claim 18 under 35 U.S.C. §102(e) as being anticipated by Rivard et al. (U.S. Patent No. 6,300,953). This rejection of these claims on this basis is traversed. Rivard fails to teach transferring texture data at a main memory access granularity, as claimed in claim 18.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

No additional fees are required for claims.

The required fee for a three month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (310) 252-7605. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

PETITION FOR EXTENSION OF TIME

Per 37 C.F.R. 1.136(a) and in connection with the Office Action mailed on THURSDAY, MARCH 20, 2003, Applicant respectfully petitions Commissioner for a three (3) month extension of time, extending the period for response to MONDAY, SEPTEMBER 22, 2003 (September 20, 2003, being a Saturday). Attached is a check in the amount of $930.00 to cover the petition filing fee for a 37 C.F.R. 1.17(a)(3) large entity. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN

Dated: September 19, 2003

By: _____
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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class Mail , With Sufficient Postage, In An Envelope Addressed To: Mail Stop Amendments, Non-Fee, Commissioner For Patents P.O. Box 1340, Alexandria, VA 22313-1450

9-19-2003
Linda Marie D'Elia September 19, 2003